CLAIMS

What is claimed is:

1. A multiplexer circuit having reduced susceptibility to single event upsets, comprising:

a plurality of input circuits, each input circuit comprising:

an input terminal,

a first pass gate coupled to the first input terminal and having a gate terminal,

a second pass gate coupled to the first pass gate and having a gate terminal, and

an output terminal coupled to the second pass gate;

a plurality of memory cells susceptible to the single event upsets, each memory cell being coupled to the gate terminal of a respective one of the pass gates in two respective different input circuits within the plurality of input circuits; and

an output node coupled to the output terminals of each of the plurality of input circuits.

2. The multiplexer circuit of Claim 1, further comprising a buffer having an input terminal, coupled to the output node, and an output terminal.

3. The multiplexer circuit of Claim 1, wherein the plurality of input circuits comprises eight input circuits.

4. The multiplexer circuit of Claim 1, wherein the first and second pass gates comprise N-channel transistors.

5. The multiplexer circuit of Claim 1, wherein exactly two of the plurality of memory cells are configured to enable their associated pass gates at any one time.

6. A multiplexer circuit having reduced susceptibility to single event upsets, comprising:

a plurality of input terminals;

an output node;

a plurality of first pass gates coupled between the plurality of input terminals and the output node, each of the first pass gates having a different associated input terminal and further having a gate terminal;

a plurality of second pass gates each coupled in series with an associated one of the first pass gates and forming therewith a pass gate pair coupled between the associated input terminal and the output node, each of the second pass gates having a gate terminal; and

a plurality of memory cells susceptible to the single event upsets, each memory cell having an output terminal coupled to the gate terminals of an associated one of the first pass gates and an associated one of the second pass gates,

wherein each of the pass gate pairs includes their associated first and second pass gates having gate terminals coupled to different ones of the memory cells, respectively.

7. The multiplexer circuit of Claim 6, further comprising a buffer having an input terminal, coupled to the output node, and an output terminal.

8. The multiplexer circuit of Claim 6, wherein the multiplexer circuit comprises eight pass gate pairs.

9. The multiplexer circuit of Claim 6, wherein the first pass gates and the second pass gates comprise N-channel transistors.

10. The multiplexer circuit of Claim 6, wherein exactly two of the plurality of memory cells are configured to enable their associated pass gates at any one time.

11. A system controlled by configuration memory cells susceptible to single event upsets, the system comprising:

a plurality of programmable logic blocks;

a plurality of interconnect lines; and

a plurality of multiplexer circuits programmably coupling the interconnect lines to each other and to the logic blocks, each of the multiplexer circuits comprising:

a plurality of input terminals;

an output node;

a plurality of first pass gates coupled between the plurality of input terminals and the output node, each of the first pass gates having a different associated input terminal and further having a gate terminal;

a plurality of second pass gates each coupled in series with an associated one of the first pass gates and forming therewith a pass gate pair coupled between the associated input terminal and the output node, each of the second pass gates having a gate terminal; and

a plurality of configuration memory cells susceptible to the single event upsets, each configuration memory cell having an output terminal coupled to the gate terminals of an associated one of the first pass gates and an associated one of the second pass gates,

wherein each of the pass gate pairs includes their associated first and second pass gates having gate terminals coupled to different ones of the plurality of configuration memory cells, respectively.

12. The system of Claim 11, each of the multiplexer circuits further comprising a buffer having an input terminal, coupled to the output node, and an output terminal.

13. The system of Claim 11, wherein each of the multiplexer circuits comprises eight pass gate pairs.

14. The system of Claim 11, wherein the first pass gates and the second pass gates comprise N-channel transistors.

15. The system of Claim 11, wherein the system comprises a programmable logic device (PLD).

16. The system of Claim 15, wherein the PLD is a field programmable gate array (FPGA) and the memory cells are static RAM cells configured with configuration data for the FPGA.

17. The system of Claim 11, wherein exactly two of the plurality of configuration memory cells are configured to enable their associated pass gates at any one time.